查询XQ4000ESERIES供应商

QPRO XQ4000E/EX QML High-Reliability FPGAs

DS021 (v2.2) June 25, 2000

Product Specification

Product Features

- Certified to MIL-PRF-38535, appendix A QML (Qualified Manufacturers Listing)
- Also available under the following Standard Microcircuit Drawings (SMD)
  - XC4005E 5962-97522
  - XC4010E 5962-97523
  - XC4013E 5962-97524
  - XC4025E 5962-97525
  - XC4028EX 5962-98509
- For more information contact the Defense Supply Center Columbus (DSCC) http://www.dscc.dla.mis/v/va/smd/smdsrch.html
- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - Synchronous write option
    - Dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution networks
- System Performance beyond 60 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12 mA sink current per XQ4000E/EX output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Backward Compatible with XC4000 Devices
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Available Speed Grades:
  - XQ4000E -3 for plastic packages only
  - -4 for ceramic packages only
  - XQ4028EX -4 for all packages

More Information

For more information refer to Xilinx XC4000E and XC4000X series Field Programmable Gate Arrays product specification. This data sheet contains pinout tables for XQ4010E only. Refer to Xilinx web site for pinout tables for other devices. (Pinouts for XQ4000E/EX are identical to XC4000E/EX.)
(http://www.xilinx.com/partinfo/databook.htm)

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Table 1: **XQ4000E/EX Field Programmable Gate Arrays**

Device	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)(1)	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. Decode Inputs per Side	Max. User I/O	Packages
XQ4005E	5,000	6,272	3,000 - 9,000	14 x 14	196	616	42	112	PG156, CB164
XQ4010E	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	60	160	PG191, CB196, HQ208
XQ4013E	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	72	192	PG223, CB228, HQ240
XQ4025E	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	96	256	PG299, CB228
XQ4028EX	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	96	256	PG299, CB228, HQ240, BG352

Notes:
1. Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

XQ4000E Switching Characteristics

XQ4000E Absolute Maximum Ratings(1)

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		–0.5 to +7.0	V
V_{IN}	Input voltage relative to GND(2)		–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to High-Z output(2)		–0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic package	+150	°C
		Plastic package	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC excursion above V_{CC} or below Ground must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to V_{CC} + 2.0V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

XQ4000E Recommended Operating Conditions(1,2)

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = –55°C to +125°C	Plastic	4.5	5.5	V
	Supply voltage relative to GND, T_C = –55°C to +125°C	Ceramic	4.5	5.5	V
V_{IH}	High-Level Input Voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-Level Input Voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement threshold are 1.5V for TTL and 2.5V for CMOS.

XQ4000E DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min	TTL outputs	2.4	-	V
	High-level output voltage @ I_{OH} = –1.0 mA, V_{CC} min	CMOS outputs	V_{CC} – 0.5	-	V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min(1)	TTL outputs	-	0.4	V
		CMOS outputs	-	0.4	V
I_{CCO}	Quiescent FPGA supply current(2)		-	50	mA
I_L	Input or output leakage current		–10	+10	µA
C_{IN}	Input capacitance (sample tested)		-	16	pF
I_{RIN}	Pad pull-up (when selected) at V_{IN} = 0V (sample tested)(3)		–0.02	–0.25	mA
I_{RLL}	Horizontal longline pull-up (when selected) at logic Low(3)		0.2	2.5	mA

Notes:
1. With 50% of the outputs simultaneously sinking 12 mA, up to a maximum of 64 pins.
2. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with the development system Tie option.
3. Characterized Only.

XQ4000E Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Note: -3 Speed Grade only applies to XQ4010E and XQ4013E Plastic Package options only. -4 Speed Grade applies to all XQ devices and is only available in Ceramic Packages only.

XQ4000E Global Buffer Switching Characteristics

Symbol	Description	Device	-3(1) Max	-4(2) Max	Units
T_{PG}	From pad through primary buffer, to any clock K	XQ4005E	-	7.0	ns
		XQ4010E	6.3	11.0	ns
		XQ4013E	6.8	11.5	ns
		XQ4025E	-	12.5	ns
T_{SG}	From pad through secondary buffer, to any clock K	XQ4005E	-	7.5	ns
		XQ4010E	6.8	11.5	ns
		XQ4013E	7.3	12.0	ns
		XQ4025E	-	13.0	ns

Notes:
1. For plastic package options only.
2. For ceramic package options only.

XQ4000E Horizontal Longline Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist.

These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

Symbol	Description	Device	-3 Max	-4 Max	Units
TBUF Driving a Horizontal Longline (LL):					
T_{IO1}	I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active.(1)	XQ4005E	-	5.0	ns
		XQ4010E	6.4	8.0	ns
		XQ4013E	7.2	9.0	ns
		XQ4025E	-	11.0	ns
T_{IO2}	I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain.(1)	XQ4005E	-	6.0	ns
		XQ4010E	6.9	10.5	ns
		XQ4013E	7.7	11.0	ns
		XQ4025E	-	12.0	ns
T_{ON}	T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.(1)	XQ4005E	-	7.0	ns
		XQ4010E	7.3	8.5	ns
		XQ4013E	7.5	8.7	ns
		XQ4025E	-	11.0	ns
T_{OFF}	T going High to TBUF going inactive, not driving LL.	XQ4005E	-	1.8	ns
		XQ4010E	1.5	1.8	ns
		XQ4013E	1.5	1.8	ns
		XQ4025E	-	1.8	ns
T_{PUS}	T going High to LL going from Low to High, pulled up by a single resistor.(1)	XQ4005E	-	23.0	ns
		XQ4010E	22.0	29.0	ns
		XQ4013E	26.0	32.0	ns
		XQ4025E	-	42.0	ns
T_{PUF}	T going High to LL going from Low to High, pulled up by two resistors.(1)	XQ4005E	-	10.0	ns
		XQ4010E	11.0	13.5	ns
		XQ4013E	13.0	15.0	ns
		XQ4025E	-	18.0	ns

Notes:
1. These values include a minimum load. Use the static timing analyzer to determine the delay for each destination.

XQ4000E Wide Decoder Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist.

These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E devices unless otherwise noted.

The following guidelines reflect worst-case values over the recommended operating conditions.

Symbol	Description[1,2]	Device	-3	-4	Units
			Max	Max	
T_{WAF}	Full length, both pull-ups, inputs from IOB I-pins	XQ4005E	-	9.5	ns
		XQ4010E	9.0	15.0	ns
		XQ4013E	11.0	16.0	ns
		XQ4025E	-	18.0	ns
T_{WAFL}	Full length, both pull-ups, inputs from internal logic	XQ4005E	-	12.5	ns
		XQ4010E	11.0	18.0	ns
		XQ4013E	13.0	19.0	ns
		XQ4025E	-	21.0	ns
T_{WAO}	Half length, one pull-up, inputs from IOB I-pins	XQ4005E	-	10.5	ns
		XQ4010E	10.0	16.0	ns
		XQ4013E	12.0	17.0	ns
		XQ4025E	-	19.0	ns
T_{WAOL}	Half length, one pull-up, inputs from internal logic	XQ4005E	-	12.5	ns
		XQ4010E	12.0	18.0	ns
		XQ4013E	14.0	19.0	ns
		XQ4025E	-	21.0	ns

Notes:

1. These delays are specified from the decoder input to the decoder output.
2. Fewer than the specified number of pull-up resistors can be used, if desired. Using fewer pull-ups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pull-ups are used.

XQ4000E CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist.

These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E devices unless otherwise noted.

Symbol	Description	-3		-4		Units
		Min	Max	Min	Max	
Combinatorial Delays						
T_{ILO}	F/G inputs to X/Y outputs	-	2.01	-	2.7	ns
T_{IHO}	F/G inputs via H to X/Y outputs	-	4.3	-	4.7	ns
T_{HH0O}	C inputs via SR through H to X/Y outputs	-	3.3	-	4.1	ns
T_{HH1O}	C inputs via H to X/Y outputs	-	3.6	-	3.7	ns
T_{HH2O}	C inputs via D_{IN} through H to X/Y outputs	-	3.6	-	4.5	ns
CLB Fast Carry Logic						
T_{OPCY}	Operand inputs (F1, F2, G1, G4) to C_{OUT}	-	2.6	-	3.2	ns
T_{ASCY}	Add/Subtract input (F3) to C_{OUT}	-	4.4	-	5.5	ns
T_{INCY}	Initialization inputs (F1, F3) to C_{OUT}	-	1.7	-	1.7	ns
T_{SUM}	C_{IN} through function generators to X/Y outputs	-	3.3	-	3.8	ns
T_{BYP}	C_{IN} to C_{OUT}, bypass function generators	-	0.7	-	1.0	ns
Sequential Delays						
T_{CKO}	Clock K to outputs Q	-	2.8	-	3.7	ns
Setup Time before Clock K						
T_{ICK}	F/G inputs	3.0	-	4.0	-	ns
T_{IHCK}	F/G inputs via H	4.6	-	6.1	-	ns
T_{HH0CK}	C inputs via H0 through H	3.6	-	4.5	-	ns
T_{HH1CK}	C inputs via H1 through H	4.1	-	5.0	-	ns
T_{HH2CK}	C inputs via H2 through H	3.8	-	4.8	-	ns
T_{DICK}	C inputs via D_{IN}	2.4	-	3.0	-	ns
T_{ECCK}	C inputs via EC	3.0	-	4.0	-	ns
T_{RCK}	C inputs via S/R, going Low (inactive)	4.0	-	4.2	-	ns
T_{CCK}	C_{IN} input via F/G	2.1	-	2.5	-	ns
T_{CHCK}	C_{IN} input via F/G and H	3.5	-	4.2	-	ns

XQ4000E CLB Switching Characteristic Guidelines *(continued)*

Symbol	Description	-3		-4		Units
		Min	Max	Min	Max	
Hold Time after Clock K						
T_{CKI}	F/G inputs	0	-	0	-	ns
T_{CKIH}	F/G inputs via H	0	-	0	-	ns
T_{CKHH0}	C inputs via H0 through H	0	-	0	-	ns
T_{CKHH1}	C inputs via H1 through H	0	-	0	-	ns
T_{CKHH2}	C inputs via H2 through H	0	-	0	-	ns
T_{CKDI}	C inputs via DIN/H2	0	-	0	-	ns
T_{CKEC}	C inputs via EC	0	-	0	-	ns
T_{CKR}	C inputs via SR, going Low (inactive)	0	-	0	-	ns
Clock						
T_{CH}	Clock High time	4.0	-	4.5	-	ns
T_{CL}	Clock Low time	4.0	-	4.5	-	ns
Set/Reset Direct						
T_{RPW}	Width (High)	4.0	-	5.5	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	4.0	-	6.5	ns
Master Set/Reset(1)						
T_{MRW}	Width (High or Low)	11.5	-	13.0	-	ns
T_{MRQ}	Delay from Global Set/Reset net to Q	-	18.7	-	23.0	ns
T_{MRK}	Global Set/Reset inactive to first active clock K edge	-	18.7	-	23.0	ns
F_{TOG}	Toggle Frequency(2)	-	125	-	111	MHz

Notes:
1. Timing is based on the XC4005E. For other devices see the static timing analyzer.
2. Export Control Max. flip-flop toggle rate.

XQ4000E CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E/EX devices unless otherwise noted.

Single-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

Symbol	Write Operation Description	Size	-3		-4		Units
			Min	Max	Min	Max	
T_{WCS}	Address write cycle time (clock K period)	16x2	14.4	-	15.0	-	ns
T_{WCTS}		32x1	14.4	-	15.0	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	7.2	1 ms	7.5	1 ms	ns
T_{WPTS}		32x1	7.2	1 ms	7.5	1 ms	ns
T_{ASS}	Address setup time before clock K	16x2	2.4	-	2.8	-	ns
T_{ASTS}		32x1	2.4	-	2.8	-	ns
T_{AHS}	Address hold time after clock K	16x2	0	-	0	-	ns
T_{AHTS}		32x1	0	-	0	-	ns
T_{DSS}	D_{IN} setup time before clock K	16x2	3.2	-	3.5	-	ns
T_{DSTS}		32x1	1.9	-	2.5	-	ns
T_{DHS}	D_{IN} hold time after clock K	16x2	0	-	0	-	ns
T_{DHTS}		32x1	0	-	0	-	ns
T_{WSS}	WE setup time before clock K	16x2	2.0	-	2.2	-	ns
T_{WSTS}		32x1	2.0	-	2.2	-	ns
T_{WHS}	WE hold time after clock K	16x2	0	-	0	-	ns
T_{WHTS}		32x1	0	-	0	-	ns
T_{WOS}	Data valid after clock K	16x2	8.8	-	-	10.3	ns
T_{WOTS}		32x1	10.3	-	-	11.6	ns

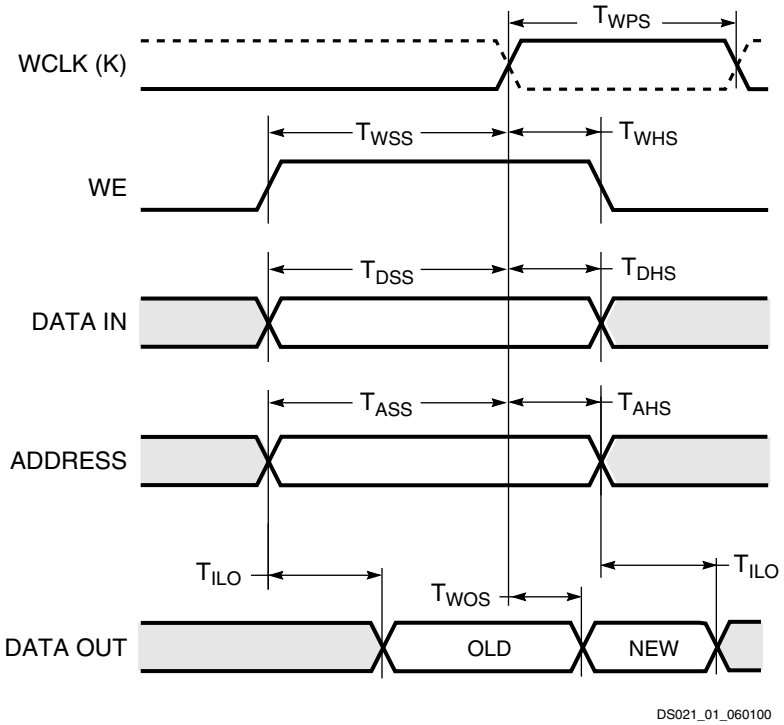
Notes:
1. Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
2. Applicable Read timing specifications are identical to Level-Sensitive Read timing.

Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

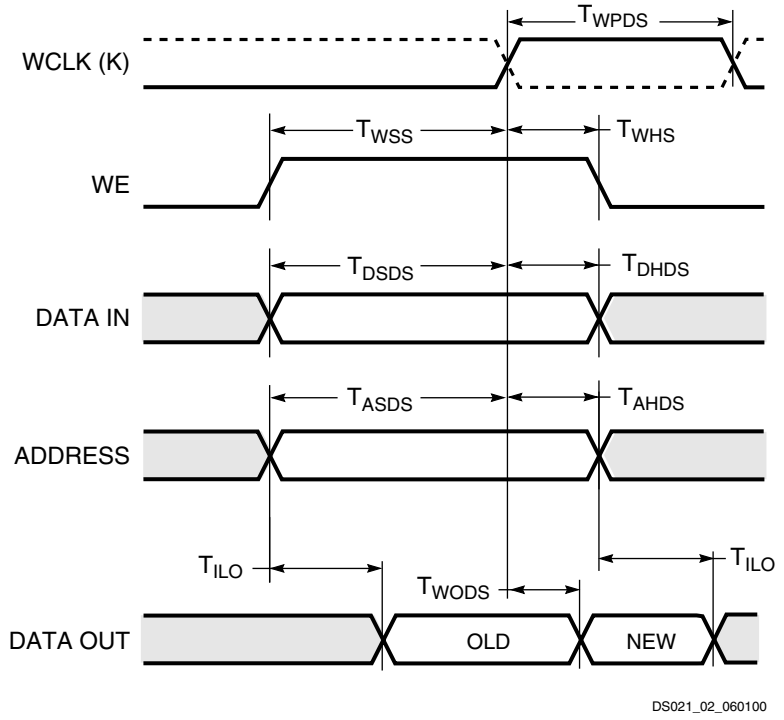
Symbol	Write Operation Description	Size[1]	-3		-4		Units
			Min	Max	Min	Max	
T_{WCDS}	Address write cycle time (clock K period)	16x1	14.4		15.0		ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	7.2	1 ms	7.5	1 ms	ns
T_{ASDS}	Address setup time before clock K	16x1	2.5	-	2.8	-	ns
T_{AHDS}	Address hold time after clock K	16x1	0	-	0	-	ns
T_{DSDS}	D_{IN} setup time before clock K	16x1	2.5	-	2.2	-	ns
T_{DHDS}	D_{IN} hold time after clock K	16x1	0	-	0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	1.8	-	2.2	-	ns
T_{WHDS}	WE hold time after clock K	16x1	0	-	0.3	-	ns
T_{WODS}	Data valid after clock K	16x1	-	7.8	-	10.0	ns

Notes:
1. Applicable Read timing specifications are identical to Level-Sensitive Read timing.

XQ4000E CLB RAM Synchronous (Edge-Triggered) Write Timing Waveform



XQ4000E CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing Waveform



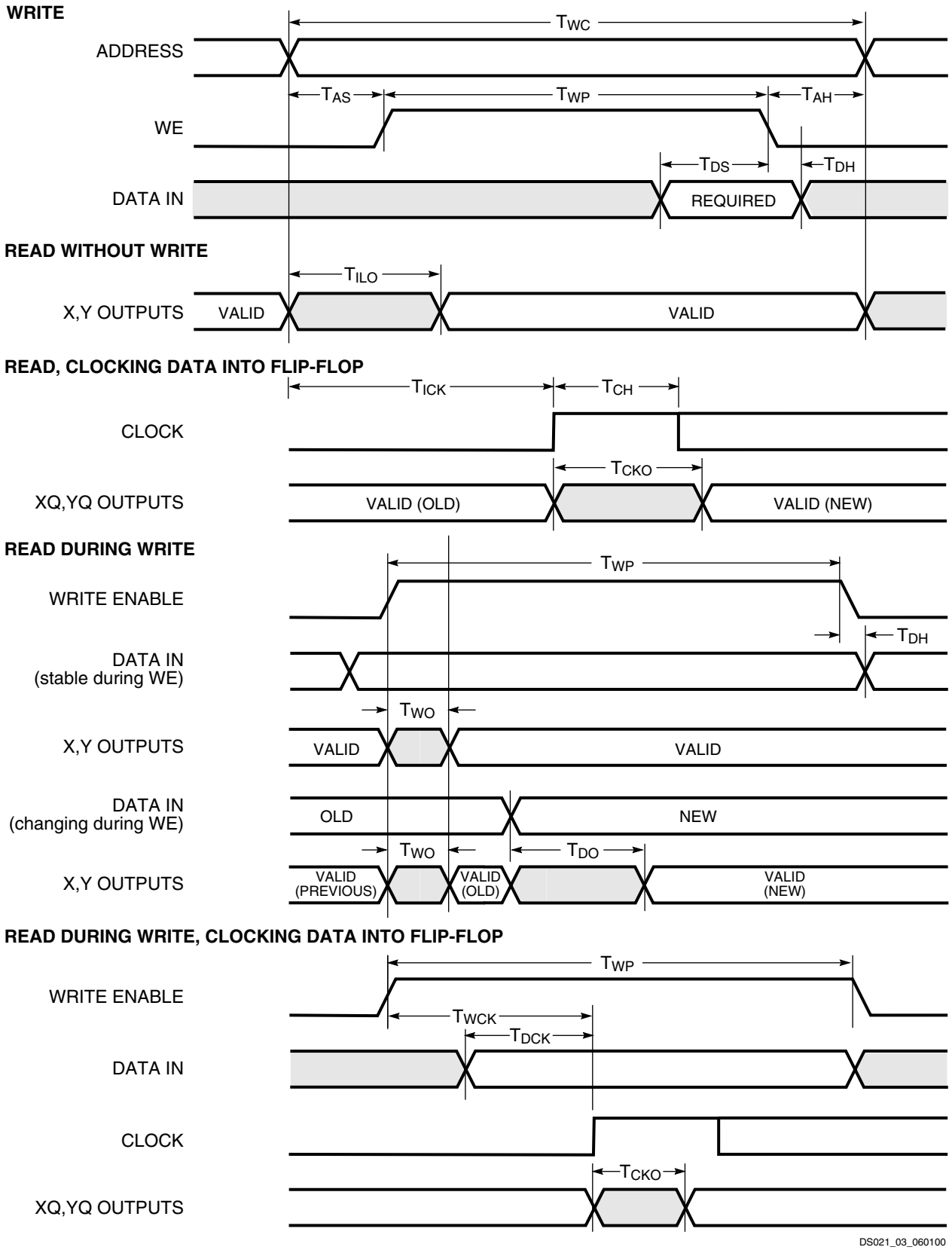
XQ4000E CLB Level-Sensitive RAM Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000E devices unless otherwise noted.

Symbol	Single Port RAM	Size	-3		-4		Units
			Min	Max	Min	Max	
Write Operation							
T_{WC}	Address write cycle time	16x2	8.0	-	8.0	-	ns
T_{WCT}		32x1	8.0	-	8.0	-	ns
T_{WP}	Write Enable pulse width (High)	16x2	4.0	-	4.0	-	ns
T_{WPT}		32x1	4.0	-	4.0	-	ns
T_{AS}	Address setup time before WE	16x2	2.0	-	2.0	-	ns
T_{AST}		32x1	2.0	-	2.0	-	ns
T_{AH}	Address hold time after end of WE	16x2	2.0	-	2.5	-	ns
T_{AHT}		32x1	2.0	-	2.0	-	ns
T_{DS}	D_{IN} setup time before end of WE	16x2	2.2	-	4.0	-	ns
T_{DST}		32x1	2.2	-	5.0	-	ns
T_{DH}	D_{IN} hold time after end of WE	16x2	2.0	-	2.0	-	ns
T_{DHT}		32x1	2.0	-	2.0	-	ns
Read Operation							
T_{RC}	Address read cycle time	16x2	3.1	-	4.5	-	ns
T_{RCT}		32x1	5.5	-	6.5	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	1.8	-	2.7	ns
T_{IHO}		32x1	-	3.2	-	4.7	ns
Read Operation, Clocking Data into Flip-Flop							
T_{ICK}	Address setup time before clock K	16x2	3.0	-	4.0	-	ns
T_{IHCK}		32x1	4.6	-	6.1	-	ns
Read During Write							
T_{WO}	Data valid after WE goes active (D_{IN} stable before WE)	16x2	-	6.0	-	10.0	ns
T_{WOT}		32x1	-	7.3	-	12.0	ns
T_{DO}	Data valid after D_{IN} (D_{IN} changes during WE)	16x2	-	6.6	-	9.0	ns
T_{DOT}		32x1	-	7.6	-	11.0	ns
Read During Write, Clocking Data into Flip-Flop							
T_{WCK}	WE setup time before clock K	16x2	6.0	-	8.0	-	ns
T_{WCKT}		32x1	6.8	-	9.6	-	ns
T_{DCK}	Data setup time before clock K	16x2	5.2	-	7.0	-	ns
T_{DOCK}		32x1	6.2	-	8.0	-	ns

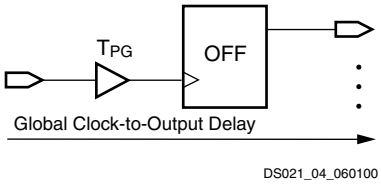
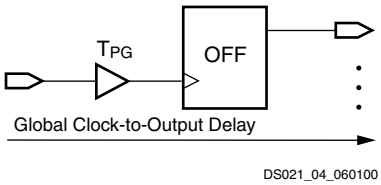
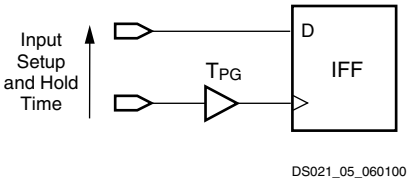
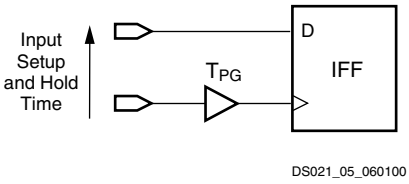
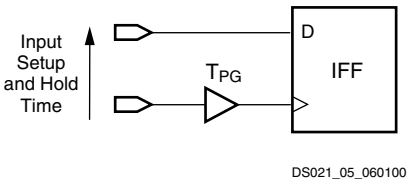
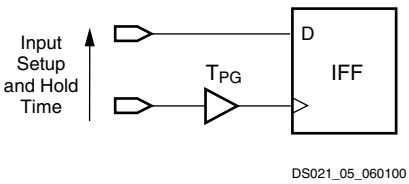
Notes:
1. Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XQ4000E CLB Level-Sensitive RAM Timing Characteristics



XQ4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL I/O)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000E devices unless otherwise noted.

Symbol	Description	Device	-3	-4	Units
T_{ICKOF} (Max)	Global clock to output (fast) using OFF 	XQ4005E	-	14.0	ns
		XQ4010E	10.9	16.0	ns
		XQ4013E	11.0	16.5	ns
		XQ4025E	-	17.0	ns
T_{ICKO} (Max)	Global clock to output (slew-limited) using OFF 	XQ4005E	-	18.0	ns
		XQ4010E	14.9	20.0	ns
		XQ4013E	15.0	20.5	ns
		XQ4025E	-	21.0	ns
T_{PSUF} (Min)	Input setup time, using IFF (no delay) 	XQ4005E	-	2.0	ns
		XQ4010E	0.2	1.0	ns
		XQ4013E	0	0.5	ns
		XQ4025E	-	0	ns
T_{PHF} (Min)	Input hold time, using IFF (no delay) 	XQ4005E	-	4.6	ns
		XQ4010E	5.5	6.0	ns
		XQ4013E	6.5	7.0	ns
		XQ4025E	-	8.0	ns
T_{PSU} (Min)	Input setup time, using IFF (with delay) 	XQ4005E	-	8.5	ns
		XQ4010E	7.0	8.5	ns
		XQ4013E	7.0	8.5	ns
		XQ4025E	-	9.5	ns
T_{PH} (Min)	Input hold time, using IFF (with delay) 	XQ4005E	-	0	ns
		XQ4010E	0	0	ns
		XQ4013E	0	0	ns
		XQ4025E	-	0	ns

Notes:
1. OFF = Output Flip-Flop
2. IFF = Input Flip-Flop or Latch

XQ4000E IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000E devices unless otherwise noted.

Symbol	Description	Device	-3		-4		Units
			Min	Max	Min	Max	
Propagation Delays (TTL Inputs)(1)							
T_{PID}	Pad to I1, I2	All devices	-	2.5	-	3.0	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	3.6	-	4.8	ns
T_{PDLI}	Pad to I1, I2 via transparent FCL and input latch, with delay	XQ4005E	-	-	-	10.8	ns
		XQ4010E	-	10.8	-	11.0	ns
		XQ4013E	-	11.2	-	11.4	ns
		XQ4025E	-	-	-	13.8	ns
Propagation Delays (CMOS Inputs)(1)							
T_{PIDC}	Pad to I1, I2	All devices	-	4.1	-	5.5	ns
T_{PLIC}	Pad to I1, I2 via transparent input latch, no delay	All devices	-	8.8	-	6.8	ns
T_{PDLIC}	Pad to I1, I2 via transparent FCL and input latch, with delay	XQ4005E	-	-	-	16.5	ns
		XQ4010E	-	14.0	-	17.5	ns
		XQ4013E	-	14.4	-	18.0	ns
		XQ4025E	-	-	-	20.8	ns
Propagation Delays (TTL Inputs)							
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	All devices	-	2.8	-	5.6	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	All devices	-	4.0	-	6.2	ns
Hold Times(2)							
T_{IKPI}	Pad to clock (IK), no delay	All devices	0	-	0	-	ns
T_{IKPID}	Pad to clock (IK), with delay	All devices	0	-	0	-	ns
T_{IKEC}	Clock enable (EC) to clock (K), no delay	All devices	1.5	-	1.5	-	ns
T_{IKECD}	Clock enable (EC) to clock (K), with delay	All devices	0	-	0	-	ns

Notes:

1. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XQ4000E IOB Input Switching Characteristic Guidelines *(continued)*

Symbol	Description	Device	-3		-4		Units
			Min	Max	Min	Max	
Setup Times (TTL Inputs)(1,2)							
T_{PICK}	Pad to clock (IK), no delay	All devices	2.6	-	4.0	-	ns
T_{PICKD}	Pad to clock (IK), with delay	XQ4005E	-	-	10.9	-	ns
		XQ4010E	9.8	-	11.3	-	ns
		XQ4013E	10.2	-	11.8	-	ns
		XQ4025E	-	-	14.0	-	ns
Setup Times (CMOS Inputs)(1,2)							
T_{PICKC}	Pad to clock (IK), no delay	All devices	3.3	-	6.0	-	ns
T_{PICKDC}	Pad to clock (IK), with delay	XQ4005E	-	-	12.0	-	ns
		XQ4010E	10.5	-	13.0	-	ns
		XQ4013E	10.9	-	13.5	-	ns
		XQ4025E	-	-	16.0	-	ns
(TTL or CMOS)							
T_{ECIK}	Clock enable (EC) to clock (IK), no delay	All devices	2.5	-	3.5	-	ns
T_{ECIKD}	Clock enable (EC) to clock (IK), with delay	XQ4005E	-	-	10.4	-	ns
		XQ4010E	9.7	-	10.7	-	ns
		XQ4013E	10.1	-	11.1	-	ns
		XQ4025E	-	-	14.0	-	ns
Global Set/Reset(3)							
T_{RRI}	Delay from GSR net through Q to I1, I2	All devices	-	7.8	-	12.0	ns
T_{MRW}	GSR width	All devices	11.5	-	13.0	-	ns
T_{MRI}	GSR inactive to first active clock (IK) edge	All devices	11.5	-	13.0	-	ns

Notes:

1. Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.
3. Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XQ4000E IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XQ4000E devices unless otherwise noted.

Symbol	Description	-3		-4		Units
		Min	Max	Min	Max	
Propagation Delays (TTL Output Levels)						
T_{OKPOF}	Clock (OK) to pad, fast	-	6.5	-	7.5	ns
T_{OKPOS}	Clock (OK) to pad, slew-rate limited	-	9.5	-	11.5	ns
T_{OPF}	Output (O) to pad, fast	-	5.5	-	8.0	ns
T_{OPS}	Output (O) to pad, slew-rate limited	-	8.6	-	12.0	ns
T_{TSHZ}	3-state to pad High-Z, slew-rate independent	-	4.2	-	10.0	ns
T_{TSONF}	3-state to pad active and valid, fast	-	8.1	-	10.0	ns
T_{TSONS}	3-state to pad active and valid, slew-rate limited	-	11.1	-	13.7	ns
Propagation Delays (CMOS Output Levels)						
T_{OKPOFC}	Clock (OK) to pad, fast	-	7.8	-	9.5	ns
T_{OKPOSC}	Clock (OK) to pad, slew-rate limited	-	11.6	-	13.5	ns
T_{OPFC}	Output (O) to pad, fast	-	9.7	-	10.0	ns
T_{OPSC}	Output (O) to pad, slew-rate limited	-	13.4	-	14.0	ns
T_{TSHZC}	3-state to pad High-Z, slew-rate independent	-	4.3	-	5.2	ns
T_{TSONFC}	3-state to pad active and valid, fast	-	7.6	-	9.1	ns
T_{TSONSC}	3-state to pad active and valid, slew-rate limited	-	11.4	-	13.1	ns
Setup and Hold Times						
T_{OOK}	Output (O) to clock (OK) setup time	4.6	-	5.0	-	ns
T_{OKO}	Output (O) to clock (OK) hold time	0	-	0	-	ns
T_{ECOK}	Clock enable (EC) to clock (OK) setup	3.5	-	4.8	-	ns
T_{OKEC}	Clock enable (EC) to clock (OK) hold	1.2	-	1.2	-	ns
Clock						
T_{CH}	Clock High	4.0	-	4.5	-	ns
T_{CL}	Clock Low	4.0	-	4.5	-	ns
Global Set/Reset(3)						
T_{RRO}	Delay from GSR net to pad	-	11.8	-	15.0	ns
T_{MRW}	GSR width	11.5	-	13.0	-	ns
T_{MRO}	GSR inactive to first active clock (OK) edge	11.5	-	13.0	-	ns

Notes:

1. Output timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section on the Xilinx web site, www.xilinx.com/partinfo/databook.htm.
2. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.
3. Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E Boundary Scan (JTAG) Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF-S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

		-3		-4		
Symbol	**Description**	**Min**	**Max**	**Min**	**Max**	**Units**
Setup Times						
T_{TDITCK}	Input (TDI) to clock (TCK)	30.0		30.0		ns
T_{TMSTCK}	Input (TMS) to clock (TCK)	15.0		15.0		ns
Hold Times						
T_{TCKTDI}	Input (TDI) to clock (TCK)	0		0		ns
T_{TCKTMS}	Input (TMS) to clock (TCK)	0		0		ns
Propagation Delay						
T_{TCKPO}	Clock (TCK) to pad (TDO)		30.0		30.0	ns
Clock						
T_{TCKH}	Clock (TCK) High	5.0		5.0		ns
T_{TCKL}	Clock (TCK) Low	5.0		5.0		ns
F_{MAX}	Frequency		15.0		15.0	MHz

Notes:

1. Input setup and hold times and clock-to-pad times are specified with respect to external signal pins.
2. Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XC4000 Data” section of the Programmable Logic Data Book.
3. Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XQ4028EX Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the A.C. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions.

All specifications subject to change without notice.

XQ4028EX Absolute Maximum Ratings(1)

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		–0.5 to +7.0	V
V_{IN}	Input voltage relative to GND(2)		–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to High-Z output(2)		–0.5 to V_{CC} + 0.5	V
V_{CCt}	Longest supply voltage rise time from 1V to 4V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic package	+150	°C
		Plastic package	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Maximum DC excursion above V_{CC} or below Ground must be limited to either 0.5V or 10 mA, whichever is easier to achieve. Maximum total combined current on all dedicated inputs and Tri-state outputs must not exceed 200 mA. During transitions, the device pins may undershoot to –2.0V or overshoot toV_{CC} +2.0V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

XQ4028EX Recommended Operating Conditions(1)

Symbol	Descriptiont		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = –55°C to +125°C	Plastic	4.5	5.5	V
	Supply voltage relative to GND, T_C = –55°C to +125°C	Ceramic	4.5	5.5	V
V_{IH}	High-level input voltage(2)	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time		-	250	ns

Notes:
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Input and output measurement threshold are 1.5V for TTL and 2.5V for CMOS.

XQ4028EX DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage at I_{OH} = –4 mA, V_{CC} min	TTL outputs	2.4	-	V
	High-level output voltage at I_{OH} = –1 mA	CMOS outputs	V_{CC} – 0.5	-	V
V_{OL}	Low-level output voltage at I_{OL} = 12 mA, V_{CC} min(1)	TTL outputs	-	0.4	V
		CMOS outputs	-	0.4	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)		3.0	-	V
I_{CCO}	Quiescent FPGA supply current(2)		-	25	mA
I_L	Input or output leakage current		–10	10	µA
C_{IN}	Input capacitance (sample tested)	Plastic packages	-	10	V
		Ceramic packages	-	16	V
I_{RPU}	Pad pull-up (when selected) at V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) at V_{IN} = 5.5V (sample tested)		0.02	0.25	mA
I_{RLL}	Horizontal longline pull-up (when selected) at logic Low(3)		0.3	2.0	mA

Notes:
1. With up to 64 pins simultaneously sinking 12 mA.
2. With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND.

XQ4028EX Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature)

Global Buffer Switching Characteristics.

Symbol	Description	-4 Max	Units
T_{GLS}	From pad through Global Low Skew buffer, to any clock K	9.2	ns
T_{GE}	From pad through Global Early buffer, to any clock K in same quadrant	5.7	ns

XQ4028EX Horizontal Longline Switching Characteristic Guidelines

Symbol	Description	-4 Max	Units
TBUF Driving a Horizontal Longline			
T_{IO1}	I going High or Low to horizontal longline going High or Low, while T is Low. Buffer is constantly active.	13.7	ns
T_{ON}	T going Low to horizontal longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	14.7	ns
TBUF Driving Half a Horizontal Longline			
T_{HIO1}	I going High or Low to half of a horizontal longline going High or Low, while T is Low. Buffer is constantly active.	6.3	ns
T_{HON}	T going Low to half of a horizontal longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	7.2	ns

Notes:
1. These values include a minimum load of one output, spaced as far as possible from the activated pull-up(s). Use the static timing analyzer to determine the delay for each destination.

XQ4028EX CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

CLB Switching Characteristics

Symbol	Description	-4		Units
		Min	Max	
Combinatorial Delays				
T_{ILO}	F/G inputs to X/Y outputs	-	2.2	ns
T_{IHO}	F/G inputs via H' to X/Y outputs	-	3.8	ns
T_{ITO}	F/G inputs via transparent latch to Q outputs	-	3.2	ns
T_{HH0O}	C inputs via SR/H0 via H to X/Y outputs	-	3.6	ns
T_{HH1O}	C inputs via H1 via H to X/Y outputs	-	3.0	ns
T_{HH2O}	C inputs via DIN/H2 via H to X/Y outputs	-	3.6	ns
T_{CBYP}	C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	-	2.0	ns
CLB Fast Carry Logic				
T_{OPCY}	Operand inputs (F1, F2, G1, G4) to C_{OUT}	-	2.5	ns
T_{ASCY}	Add/Subtract input (F3) to C_{OUT}	-	4.1	ns
T_{INCY}	Initialization inputs (F1, F3) to C_{OUT}	-	1.9	ns
T_{SUM}	C_{IN} through function generators to X/Y outputs	-	3.0	ns
T_{BYP}	C_{IN} to C_{OUT}, bypass function generators	-	0.60	ns
T_{NET}	Carry net selay, C_{OUT} to C_{IN}	-	0.18	ns
Sequential Delays				
T_{CKO}	Clock K to flip-flop outputs Q	-	2.2	ns
T_{CKLO}	Clock K to latch outputs Q	-	2.2	ns
Setup Time before Clock K				
T_{ICK}	F/G inputs	1.3	-	ns
T_{IHCK}	F/G inputs via H	3.0	-	ns
T_{HH0CK}	C inputs via H0 through H	2.8	-	ns
T_{HH1CK}	C inputs via H1 through H	2.2	-	ns
T_{HH2CK}	C inputs via H2 through H	2.8	-	ns
T_{DICK}	C inputs via DIN	1.2	-	ns
T_{ECCK}	C inputs via EC	1.2	-	ns
T_{RCK}	C inputs via S/R, going Low (inactive)	0.8	-	ns
T_{CCK}	CIN input via F/G	2.2	-	ns
T_{CHCK}	CIN input via F/G and H	3.9	-	ns
Hold Time after Clock K				
T_{CKI}	F/G inputs	0	-	ns

CLB Switching Characteristics *(Continued)*

Symbol	Description	-4		Units
		Min	Max	
T_{CKIH}	F/G inputs via H	0	-	ns
T_{CKHH0}	C inputs via SR/H0 through H	0	-	ns
T_{CKHH1}	C inputs via H1 through H	0	-	ns
T_{CKHH2}	C inputs via DIN/H2 through H	0	-	ns
T_{CKDI}	C inputs via DIN/H2	0	-	ns
T_{CKEC}	C inputs via EC	0	-	ns
T_{CKR}	C inputs via SR, going Low (inactive)	0	-	ns
Clock				
T_{CH}	Clock High time	3.5	-	ns
T_{CL}	Clock Low time	3.5	-	ns
Set/Reset Direct				
T_{RPW}	Width (High)	3.5	-	ns
T_{RIO}	Delay from C inputs via S/R, going High to Q	-	4.5	ns
Global Set/Reset				
T_{MRW}	Minimum GSR pulse width	-	13.0	ns
T_{MRQ}	Delay from GSR input to any Q	-	22.8	
F_{TOG}	Toggle frequency (MHz) (for export control)	-	143	MHz

XQ4028EX CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

Symbol	Single Port RAM	Size	-4		Units
			Min	Max	
Write Operation					
T_{WCS}	Address write cycle time (clock K period)	16x2	11.0	-	ns
T_{WCTS}		32x1	11.0	-	ns
T_{WPS}	Clock K pulse width (active edge)	16x2	5.5	-	ns
T_{WPTS}		32x1	5.5	-	ns
T_{ASS}	Address setup time before clock K	16x2	2.7	-	ns
T_{ASTS}		32x1	2.6	-	ns
T_{AHS}	Address hold time after clock K	16x2	0	-	ns
T_{AHTS}		32x1	0	-	ns
T_{DSS}	DIN setup time before clock K	16x2	2.4	-	ns
T_{DSTS}		32x1	2.9	-	ns
T_{DHS}	DIN hold time after clock K	16x2	0	-	ns
T_{DHTS}		32x1	0	-	ns
T_{WSS}	WE setup time before clock K	16x2	2.3	-	ns
T_{WSTS}		32x1	2.1	-	ns
T_{WHS}	WE hold time after clock K	16x2	0	-	ns
T_{WHTS}		32x1	0	-	ns
T_{WOS}	Data valid after clock K	16x2	-	8.2	ns
T_{WOTS}		32x1	-	10.1	ns

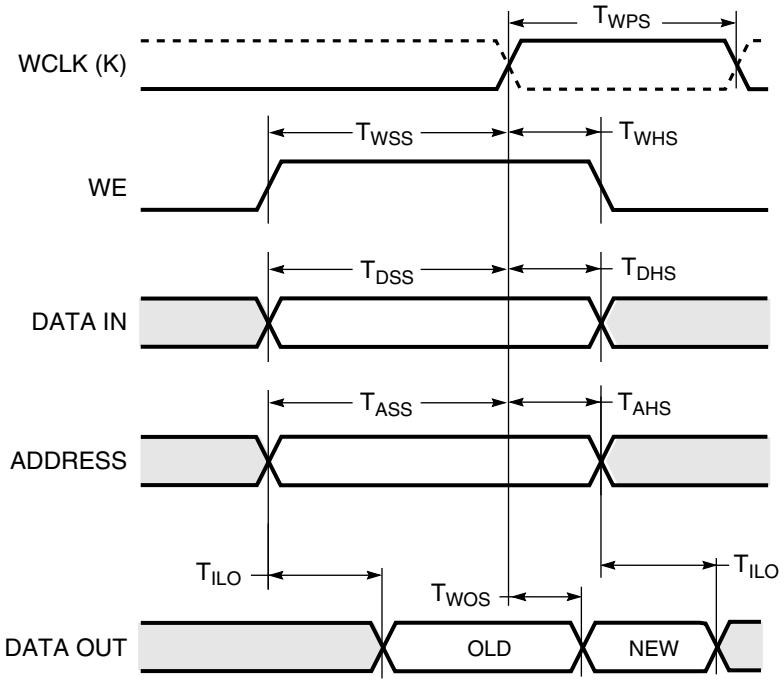
Notes:
1. Applicable Read timing specifications are identical to Level-Sensitive Read timing.

Dual-Port RAM Synchronous (Edge-Triggered) Write Operation Characteristics

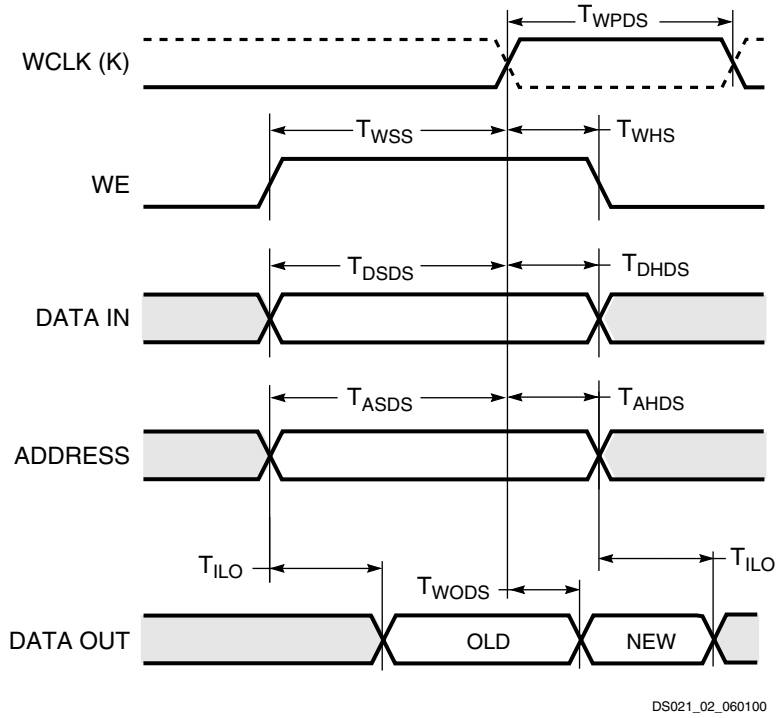
Symbol	Dual Port RAM	Size[1]	-4		Units
			Min	Max	
Write Operation					
T_{WCDS}	Address write cycle time (clock K period)	16x1	11.0		ns
T_{WPDS}	Clock K pulse width (active edge)	16x1	5.5	-	ns
T_{ASDS}	Address setup time before clock K	16x1	3.1	-	ns
T_{AHDS}	Address hold time after clock K	16x1	0	-	ns
T_{DSDS}	DIN setup time before clock K	16x1	2.9	-	ns
T_{DHDS}	DIN hold time after clock K	16x1	0	-	ns
T_{WSDS}	WE setup time before clock K	16x1	2.1	-	ns
T_{WHDS}	WE hold time after clock K	16x1	0	-	ns
T_{WODS}	Data valid after clock K	16x1	-	9.4	ns

Notes:
1. Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
2. Applicable Read timing specifications are identical to Level-Sensitive Read timing.

XQ4028EX CLB RAM Synchronous (Edge-Triggered) Write Timing Waveform



XQ4028EX CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing Waveform



XQ4028EX CLB RAM Asynchronous (Level-Sensitive) Write and Read Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

Symbol	Single Port RAM	Size	-4		Units
			Min	Max	
Write Operation					
T_{WC}	Address write cycle time	16x2	10.6	-	ns
T_{WCT}		32x1	10.6	-	ns
T_{WP}	Write Enable pulse width (High)	16x2	5.3	-	ns
T_{WPT}		32x1	5.3	-	ns
T_{AS}	Address setup time before WE	16x2	2.8	-	ns
T_{AST}		32x1	2.8	-	ns
T_{AH}	Address hold time after end of WE	16x2	1.7	-	ns
T_{AHT}		32x1	1.7	-	ns
T_{DS}	DIN setup time before end of WE	16x2	1.1	-	ns
T_{DST}		32x1	1.1	-	ns
T_{DH}	DIN hold time after end of WE	16x2	6.6	-	ns
T_{DHT}		32x1	6.6	-	ns
Read Operation					
T_{RC}	Address read cycle time	16x2	4.5	-	ns
T_{RCT}		32x1	6.5	-	ns
T_{ILO}	Data valid after address change (no Write Enable)	16x2	-	2.2	ns
T_{IHO}		32x1	-	3.8	ns
Read Operation, Clocking Data into Flip-Flop					
T_{ICK}	Address setup time before clock K	16x2	1.5	-	ns
T_{IHCK}		32x1	3.2	-	ns
Read During Write					
T_{WO}	Data valid after WE goes active (DIN stable before WE)	16x2	-	6.5	ns
T_{WOT}		32x1	-	7.4	ns
T_{DO}	Data valid after DIN (DIN changes during WE)	16x2	-	7.7	ns
T_{DOT}		32x1	-	8.2	ns
Read During Write, Clocking Data into Flip-Flop					
T_{WCK}	WE setup time before clock K	16x2	7.1	-	ns
T_{WCKT}		32x1	9.2	-	ns
T_{DCK}	Data setup time before clock K	16x2	5.9	-	ns
T_{DOCK}		32x1	8.4	-	ns

Notes:
1. Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XQ4028EX CLB Level-Sensitive RAM Timing Waveforms

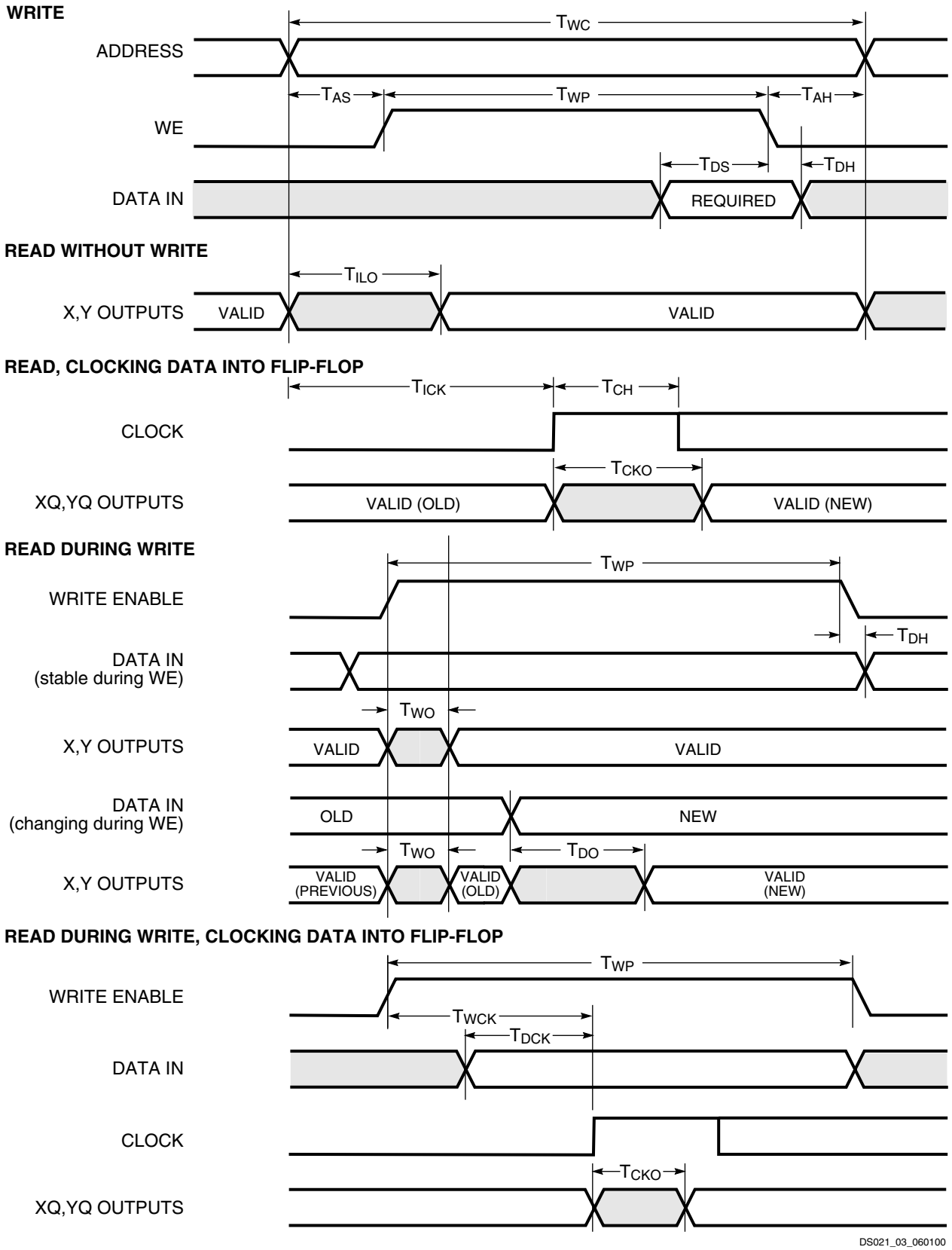


Figure 1:

XQ4028EX Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000EX devices unless otherwise noted.

XQ4028EX Output Flip-Flop, Clock to Out(1,2)

Symbol	Description	-4 Max	Units
T_{ICKOF}	Global low skew clock to output using OFF(3)	16.6	ns
T_{ICKEOF}	Global early clock to output using OFF(3)	13.1	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at TTL threshold with 50 pF external capacitive load.
3. OFF = Output Flip-Flop

XQ4028EX Output Mux, Clock to Out(1,2)

Symbol	Description	-4 Max	Units
T_{PFPF}	Global low skew clock to TTL output (fast) using OMUX3)	15.9	ns
T_{PEFPF}	Global early clock to TTL output (fast) using OMUXF(3)	12.4	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see graph below.
3. OMUX = Output MUX

XQ4028EX Output Level and Slew Rate Adjustments

The following table must be used to adjust output parameters and output switching characteristics.

Symbol	Description	-4 Max	Units
T_{TTLOF}	For TTL output FAST add	0	ns
T_{TTLO}	For TTL output SLOW add	2.9	ns
T_{CMOSOF}	For CMOS FAST output add	1.0	ns
T_{CMOSO}	For CMOS SLOW output add	3.6	ns

XQ4028EX Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XQ4000EX devices unless otherwise noted

XQ4028EX Global Low Skew Clock, Setup and Hold

Symbol	Description	-4 Min	Units
T_{PSD}	Input setup time, using Global Low Skew clock and IFF (full delay)	8.0	ns
T_{PHD}	Input hold time, using Global Low Skew clock and IFF (full delay)	0	ns

Notes:
1. IFF = Flip-Flop or Latch

XQ4028EX Global Early Clock, Setup and Hold for IFF

Symbol	Description	-4 Min(2)	Units
T_{PSEP}	Input setup time, using Global Early clock and IFF (full delay)	6.5	ns
T_{PHEP}	Input hold time, using Global Early clock and IFF (full delay)	0	ns

Notes:
1. IFF = Flip-Flop or Latch
2. Setup parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.6 ns for BUFGE #s 1, 2, 5 and 6.

XQ4028EX Global Early Clock, Setup and Hold for FCL

Symbol	Description	-4 Min(2)	Units
T_{PFSEP}	Input setup time, using Global Early clock and FCL (partial delay)	3.4	ns
T_{PFHEP}	Input hold time, using Global Early clock and FCL (partial delay)	0	ns

Notes:
1. FCL = Fast Capture Latch
2. For CMOS input levels, see the XQ4028EX Input Threshold Adjustments.
3. Setup time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time under given design conditions.
4. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.
5. Setup parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.2 ns for BUFGE #s 1, 2, 5 and 6.

XQ4028EX Input Threshold Adjustments

The following table must be used to adjust input parameters and input switching characteristics.

Symbol	Description	-4 Max	Units
T_{TTLI}	For TTL input add	0	ns
T_{CMOSI}	For CMOS input add	0.3	ns

XQ4028EX IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XQ4000EX devices unless otherwise noted.

Symbol	Description	-4	Units
		Min	
Clocks			
T_{OKIK}	Delay from FCL enable (OK) active to IFF clock (IK) active edge	3.2	ns
Propagation Delays			
T_{PID}	Pad to I1, I2	2.2	ns
T_{PLI}	Pad to I1, I2 via transparent input latch, no delay	3.8	ns
T_{PPLI}	Pad to I1, I2 via transparent input latch, partial delay	13.3	ns
T_{PDLI}	Pad to I1, I2 via transparent input latch, full delay	18.2	ns
T_{PFLI}	Pad to I1, I2 via transparent FCL and input latch, no delay	5.3	ns
T_{PPFLI}	Pad to I1, I2 via transparent FCL and input latch, partial delay	13.6	ns
Propagation Delays (TTL Inputs)			
T_{IKRI}	Clock (IK) to I1, I2 (flip-flop)	3.0	ns
T_{IKLI}	Clock (IK) to I1, I2 (latch enable, active Low)	3.2	ns
T_{OKLI}	FCL enable (OK) active edge to I1, I2 (via transparent standard input latch)	6.2	ns
Global Set/Reset			
T_{MRW}	Minimum GSR pulse width	13.0	ns
T_{RRI}	Delay from GSR input to any Q	22.8	ns

Notes:
1. FCL = Fast Capture Latch, IFF = Input Flip-Flop or Latch
2. For CMOS input levels, see the "XQ4028EX Input Threshold Adjustments" on page 28.
3. For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Setup and Hold tables on page 28.

XQ4028EX IOB Input Switching Characteristic Guidelines (Continued)

Symbol	Description	-4 Min	Units
Setup Times			
T_{PICK}	Pad to Clock (IK), no delay	2.5	ns
T_{PICKP}	Pad to Clock (IK), partial delay	10.8	ns
T_{PICKD}	Pad to Clock (IK), full delay	15.7	ns
T_{PICKF}	Pad to Clock (IK), via transparent Fast Capture Latch, no delay	3.9	ns
T_{PICKFP}	Pad to Clock (IK), via transparent Fast Capture Latch, partial delay	12.3	ns
T_{POCK}	Pad to Fast Capture Latch Enable (OK), no delay	0.8	ns
T_{POCKP}	Pad to Fast Capture Latch Enable (OK), partial delay	9.1	ns
Setup Times (TTL or CMOS Inputs)			
T_{ECIK}	Clock Enable (EC) to Clock (IK)	0.3	ns
Hold Times			
T_{IKPI}	Pad to Clock (IK), no delay	0	ns
T_{IKPIP}	Pad to Clock (IK), partial delay	0	ns
T_{IKPID}	Pad to Clock (IK), full delay	0	ns
T_{IKPIF}	Pad to Clock (IK) via transparent Fast Capture Latch, no delay	0	ns
T_{IKFPIP}	Pad to Clock (IK) via transparent Fast Capture Latch, partial delay	0	ns
T_{IKFPID}	Pad to Clock (IK) via transparent Fast Capture Latch, full delay	0	ns
T_{IKEC}	Clock Enable (EC) to Clock (IK), no delay	0	ns
T_{IKECP}	Clock Enable (EC) to Clock (IK), partial delay	0	ns
T_{IKECD}	Clock Enable (EC) to Clock (IK), full delay	0	ns
T_{OKPI}	Pad to Fast Capture Latch Enable (OK), no delay	0	ns
T_{OKPIP}	Pad to Fast Capture Latch Enable (OK), partial delay	0	ns

Notes:
1. For CMOS input levels, see the "XQ4028EX Input Threshold Adjustments" on page 28.
2. For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Setup and Hold tables on page 28.

FXQ4028EX IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XQ4000EX devices unless otherwise noted.

Symbol	Description	-4		Units
		Min	Max	
Propagation Delays (TTL Output Levels)				
T_{OKPOF}	Clock (OK) to pad, fast	-	7.4	ns
T_{OPF}	Output (O) to pad, fast	-	6.2	ns
T_{TSHZ}	3-state to pad High-Z, slew-rate independent	-	4.9	ns
T_{TSONF}	3-state to pad active and valid, fast	-	6.2	ns
T_{OKFPF}	Output MUX select (OK) to pad	-	6.7	ns
T_{CEFPF}	Fast path output MUX input (EC) to pad	-	6.2	
T_{OFPF}	Slowest path output MUX input (EC) to pad	-	7.3	
Setup and Hold Times				
T_{OOK}	Output (O) to clock (OK) setup time	0.6	-	ns
T_{OKO}	Output (O) to clock (OK) hold time	0	-	ns
T_{ECOK}	Clock enable (EC) to clock (OK) setup	0	-	ns
T_{OKEC}	Clock enable (EC) to clock (OK) hold	0	-	ns
Clocks				
T_{CH}	Clock High	3.5	-	ns
T_{CL}	Clock Low	3.5	-	ns
Global Set/Reset				
T_{MRW}	Minimum GSR pulse width	13.0	-	ns
T_{RRI}	Delay from GSR input to any pad	30.2	-	ns

Notes:
1. Output timing is measured at TTL threshold, with 35 pF external capacitive loads.
2. For CMOS output levels, see the "XQ4028EX Output Level and Slew Rate Adjustments" on page 27.

CB191/196 Package for XQ4010E

Pin Description	PG191	CB196	Bound Scan
GND	D4	P1	-
PGCK1_(A16*I/0)	C3	P2	122
I/O_(A17)	C4	P3	125
I/0	B3	P4	128
-	-	P5(1)	-
I/O	C5	P6	131
I/O_(TDI)	A2	P7	134
I/O_(TCK)	B4	P8	137
I/O	C6	P9	140
I/O	A3	P10	143
I/O	B5	P11	146
I/O	B6	P12	149
GND	C7	P13	-
I/O	A4	P14	152
I/O	A5	P15	155
I/O_(TMS)	B7	P16	158
I/O	A6	P17	161
I/O	C8	P18	164
I/O	A7	P19	167
I/O	B8	P20	170
I/O	A8	P21	173
I/O	B9	P22	176
I/O	C9	P23	179
GND	D9	P24	-
VCC	D10	P25	-
I/O	C10	P26	182
I/O	B10	P27	185
I/O	A9	P28	-
I/O	A10	P29	191
I/O	A11	P30	194
I/O	C11	P31	197
I/O	B11	P32	200
I/O	A12	P33	203
I/O	B12	P34	206
I/O	A13	P35	209
GND	C12	P36	-
I/O	B13	P37	212
I/O	A14	P38	215
I/O	A15	P39	218
I/O	C13	P40	221
I/O	B14	P41	224
I/O	A16	P42	227
I/O	B15	P43	230
I/O	C14	P44	233
I/O	A17	P45	236
SCGK2_(I/O)	B16	P46	239
M1	C15	P47	242
GND	D15	P48	-
M0	A18	P49	245(2)
VCC	D16	P50	-
M2	C16	P51	246(2)
PGCK2_(I/O)	B17	P52	247
I/O_(HDC)	E16	P53	250
-	-	P54(1)	-
I/O	C17	P55	253
I/0	D17	P56	256
I/O	B18	P57	259
I/O_(LDC)	E17	P58	262
I/O	F16	P59	265
I/O	C18	P60	268
I/O	D18	P61	271
I/O	F17	P62	274
GND	G16	P63	-
I/O	E18	P64	277
I/O	F18	P65	280
I/O	G17	P66	283
I/O	G18	P67	286

Notes:
1. Indicates unconnected package pins.
2. Contributes only one bit (.I) to the boundary scan register.
   Boundary Scan Bit 0 = TD0.T
   Boundary Scan Bit 1 = TD0.0
   Boundary Scan Bit 487 = BSCAN.UPD

Notes:
1. Indicates unconnected package pins.
2. Contributes only one bit (.I) to the boundary scan register.
   Boundary Scan Bit 0 = TD0.T
   Boundary Scan Bit 1 = TD0.0
   Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
I/O	H16	P68	286
I/O	H17	P69	291
I/O	H18	P70	295
I/O	J18	P71	298
I/O	J17	P72	301
I/O_(/ERR_/INIT)	J16	P73	304
VCC	J15	P74	-
GND	K15	P75	-
I/O	K16	P76	307
I/O	K17	P77	310
I/O	K18	P78	313
I/O	L18	P79	316
I/O	L17	P80	319
I/O	L16	P81	322
I/O	M18	P82	325
I/O	M17	P83	328
I/O	N18	P84	331
I/O	P18	P85	334
GND	M16	P86	-
I/O	N17	P87	337
I/O	R18	P88	340
I/O	T18	P89	343
I/O	P17	P90	349
I/O	N16	P91	349
I/O	T17	P92	352
I/O	R17	P93	355
I/O	P16	P94	358
I/O	U18	P95	361
SGCK3_(I/O)	T16	P96	364
GND	R16	P97	-
DONE	U17	P98	-
VCC	R15	P99	-
/PROG	V18	P100	-
I/O_(D7)	T15	P101	367

Notes:
1. Indicates unconnected package pins.
2. Contributes only one bit (.I) to the boundary scan register.
   Boundary Scan Bit 0 = TD0.T
   Boundary Scan Bit 1 = TD0.0
   Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
PGCK3_(I/O)	U16	P102	370
-	-	P103(1)	-
I/O	T14	P104	376
I/O	U15	P105	376
I/O_(D6)	V17	P106	379
I/O	V16	P107	382
I/O	T13	P108	385
I/O	U14	P109	388
I/O	V15	P110	391
I/O	V14	P111	394
GND	T12	P112	-
I/O	U13	P113	397
I/O	V13	P114	400
I/O_(D5)	U12	P115	403
I/O_(/CSO)	V12	P116	406
I/O	T11	P117	409
I/O	U11	P118	412
I/O	V11	P119	415
I/O	V1	P120	418
I/O_(D4)	U10	P121	421
I/O	T10	P122	424
VCC	R10	P123	-
GND	R9	P124	-
I/O_(D3)	T9	P125	427
I/O_(/RS)	U9	P126	430
I/O	V9	P127	433
I/O	V8	P128	436
I/O	U8	P129	439
I/O	T8	P130	442
I/O_(D2)	V7	P131	445
I/O	U7	P132	448
I/O	V6	P133	451
I/O	U6	P134	454
GND	T7	P135	-

Notes:
1. Indicates unconnected package pins.
2. Contributes only one bit (.I) to the boundary scan register.
   Boundary Scan Bit 0 = TD0.T
   Boundary Scan Bit 1 = TD0.0
   Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
I/O	V5	P136	457
I/O	V4	P137	460
I/O	U5	P138	463
I/O	T6	T139	446
I/O_(D1)	V3	P140	469
I/O_(RCLK-/BUSY/RDY)	V2	P141	472
I/O	U4	P142	475
I/O	T5	P143	478
I/O_(D0*_DIN)	U3	P144	481
SGCK4_(DOUT*_I/O)	T4	P145	484
CCLK	V1	P146	-
VCC	R4	P147	-
TDO	U2	P148	-
GND	R3	P149	-
I/O_(A0*_WS)	T3	P150	2
PGCK4_(I/O*_A1)	U1	P151	5
-	-	P152(1)	-
I/O	P3	P153	8
I/O	R2	P154	11
I/O_(CS1*_A2)	T2	P155	14
I/O_(A3)	N3	P156	17
I/O	P2	P157	20
I/O	T1	P158	23
I/O	R1	P159	26
I/O	N2	P160	29
GND	M3	P161	-
I/O	P1	P162	32
I/O	N1	P163	35
I/O_(A4)	M2	P164	38
I/O_(A5)	M1	P165	41
I/O	L3	P166	44
I/O	L2	P167	47
I/O	L1	P168	50

Notes:
1. Indicates unconnected package pins.
2. Contributes only one bit (.I) to the boundary scan register.
   Boundary Scan Bit 0 = TD0.T
   Boundary Scan Bit 1 = TD0.0
   Boundary Scan Bit 487 = BSCAN.UPD

Pin Description	PG191	CB196	Bound Scan
I/O	K1	P169	53
I/O_(A6)	K2	P170	56
I/O_(A7)	K3	P171	59
GND	K4	P172	-
VCC	J4	P173	-
I/O_(A8)	J3	P174	62
I/O_(A9)	J2	P175	65
I/O	J1	P176	68
I/O	H1	P177	71
I/O	H2	P178	74
I/O	H3	P179	77
I/O_(A10)	G1	P180	80
I/O_(A11)	G2	P181	83
I/O	F1	P182	86
I/O	E1	P183	89
GND	G3	P184	-
I/O	F2	P185	92
I/O	D1	P186	96
I/O	C1	P187	98
I/O	E2	P188	101
I/O_(A12)	F3	P189	104
I/O_(A13	D2	P190	107
-	-	P192(1)	-
I/O	E3	P193	113
I/O_(A14)	C2	P194	116
SGCK1(A15*I/O)	B2	P195	119
VCC	D3	P196	-

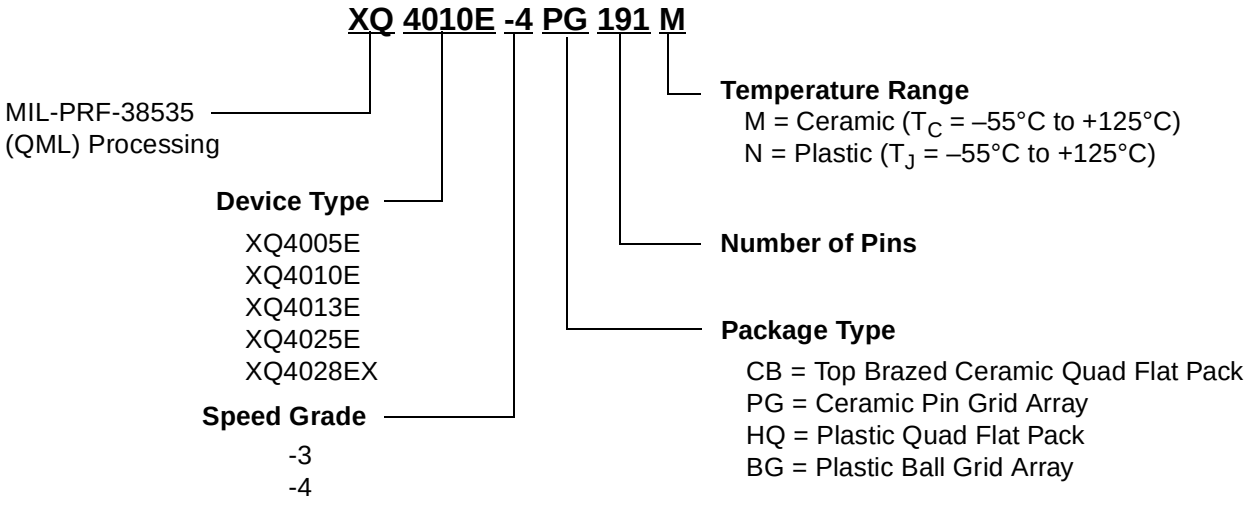
Notes:
1. Indicates unconnected package pins.
2. Contributes only one bit (.I) to the boundary scan register.
   Boundary Scan Bit 0 = TD0.T
   Boundary Scan Bit 1 = TD0.0
   Boundary Scan Bit 487 = BSCAN.UPD

Additional XQ4010E Package Pins

CB196

No Connect Pins			
P5	P54	P103	P152
P192	-	-	-

Ordering Information



Revision History

The following table shows the revision history for this document

Date	Version	Description
05/19/98	2.1	Updates.
06/25/00	2.2	Updated timing specifications to match with commercial data sheet. Updated format.